DESIGN-ORIENTED NON-LINEAR ANALYSIS OF CLASS-AB POWER AMPLIFIERS

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ABSTRACT

In this work an efficient and reliable non-linear analysis method is proposed for the analysis and design of high-efficiency power amplifiers operating in any class. On the basis of a simplified device model, the method can be used for the optimization of efficiency, output power and drive level of a power stage. Its feasibility is demonstrated comparing the method with the results of a more elaborate non-linear CAD analysis program and with experimental data.

INTRODUCTION

High power, high efficiency narrowband power amplifiers are key elements in most communication systems, where low DC power is available or difficulties are associated with heat removal. Their successful design involves the careful choice of bias points (operating class), drive level and loading. In order to analyze and successively optimize the performance of the power stage, output power, gain, efficiency and harmonic distortion must be qualitatively and quantitatively evaluated.

A fast and accurate analysis method must therefore be available to the designer. Commercially available nonlinear simulation tools [1-3] are highly accurate and resonably fast, but the time required for each analysis of a nonlinear amplifier is too long to allow a systematic investigation or an iterative optimization. Simplified methods already presented [4-8] do not allow the analysis and the optimization of the nonlinear amplifier behaviour over the whole operating range (i.e. at breakdown or current saturation). On the other hand, Load-Pull methods are often cumbersome and inaccurate [9].

The method proposed here overcomes the previously mentioned limitations via a simplified but fully non-linear analysis; this method can be used for the optimization of a class-A,AB,B or C power stage via design tables and guidelines.

THE ANALYSIS METHOD

Our assumption, common to many device simplified models [4-8], is to represent the internal reactances of the transistor by equivalent linear capacitances. "Output" reactances (C_{gd} and C_{ds}), in fact, exhibit a weak dependence on gate and drain voltages, and the input current through C_{gs} does not influence (in a first approximation) the amplifier's performance. C_{gd} as a feedback element may be neglected, as it has negligible effect on the optimum load determination [10]. "Average" linear capacitors can be easily deduced from small-signal measurements at many bias points and considered as parasitics.

Power amplifiers are output-matched with the conjugate of the large-signal output impedance, so to resonate the parasitic capacitances at the operating frequency; the result is a "tuned" output circuit which transfers the active power from the intrinsic transistor to the load (fig.1). We may therefore assume that voltage and current are in phase at the intrinsic drain terminal; if we also assume a perfect resonator, or alternatively a short circuit load at higher harmonics (a good assumption from the efficiency point of view), we may take the output voltage as a sinusoid. The non-linear drain-source current generator can be piecewise-linearised, and replaced by a linear voltage-controlled current generator in the saturation region, a resistance in the ohmic and breakdown regions, and an open circuit in the pinch-off region (fig.2); the different models are switched when the

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current point in the Vds-Id plane crosses the border between two regions.

For a given bias point, load resistance and drive level, the output current waveform can be determined with a Newton-based iterative procedure, whose error function can be expressed as:

$$F(m) = V_{ds}(m) - R_L \cdot I_1(m)$$

where m is the slope of the dynamic load line in the linear region, $V_{ds}(m)$ is the amplitude of the drain-source dynamic voltage, and $I_1(m)$ is the amplitude of the first harmonic component of the drain current.

After convergence has been reached, it is easy to find the Fourier expansion coefficients of the drain current (I_n), from which the DC power and the drain voltage amplitude can be computed:

$$P_{dc} = V_{dd} I_o \qquad V_{ds} = R_L I_1$$

and hence output power, gain and power added efficiency:

$$P_1 = \frac{1}{2} V_{ds} I_1 \qquad G = \frac{P_1}{P_{in}} \qquad \eta_{add} = \frac{(P_1 - P_{in})}{P_{dc}}$$

Verification with a non-linear analysis program has been carried out; in fig.3 we report the comparison between the results of Libra [1] and our simplified analysis for a 10 GHz, 21dBm class-AB power stage, based on a Plessey P35_1130 medium power MESFET, designed for best efficiency. The results are close to the ones obtained by the commercial package, showing the feasibility of the procedure. In fig. 4 the load curves from Libra are plotted, with superimposed the corresponding load line from our model. The reactive behaviour of the Libra curves is due to the internal parasitic capacitances of the device, which are accounted for in our model by means of external linear capacitances, evaluated beforehand.

As a further verification, a comparison with an experimental result from [11] is presented in fig. 5: good agreement has been obtained over the whole operating range, from the linear to saturation region.

THE DESIGN PROCEDURE

Design criteria for the optimization of bias point, load resistance and drive level of a power stage can be deduced from the simplified method.

The procedure begins with the identification of the important physical parametres from the I_d - V_{ds} characteristics (fig.2); they are: V_k (drain saturation voltage), Imax (maximum drain current at $V_{gs} = V_{bi}$), V_{bro} (drain-source breakdown voltage with $V_{gs} = 0$) and V_p (pinch-off voltage).

Another quantity to be determined is the small-signal gain of the transistor, which can be obtained implicitly through the values of C_{gs}, R_i and g_m, or explicitly from either measurements or linear simulation for a given bias point and load. The actual gain in any other condition can be analytically deduced.

The next step is the choice of the drain bias voltage as

$$V_{dc} = V_k + \frac{(V_{bro} - V_k - 2|V_{GG}| - V_{bi})}{2}$$

where V_k is as in fig.2; in fact, V_{GG} and V_k are a first guess, to be readjusted afterwards.

The choice of the optimum load and quiescent drain current is made through fig.6 and fig.7, where output power and power-added efficiency as computed from the model are plotted vs. R_L, with normalized quiescent current as a parameter. Those values are evaluated for the drive level corresponding, for each point, to maximum efficiency. The behaviour of the efficiency is strongly influenced by the gain of the transistor; we have therefore reported two cases for 15dB and 9dB small-signal gain.

The plots are done for values of the load corresponding to the region where the best compromise between output power and power-added efficiency can be made. It is easily seen from the plot that for increasing load resistance, the output power decreases, but power-added efficiency increases because of the prevailing effect of the increased gain: the best compromise between the two is left to the designer. It is also apparent from the plots that the output power is weakly dependent on the bias current, while the power-added

efficiency is much more dependent on it; in particular the two contrasting effects of decreasing DC power dissipation and decreasing gain (going from class-A to class-B) produce a clear maximum. Here again the choice of the compromise between best output power and best efficiency is left to the designer. We remark that the choice is influenced by the magnitude of the small-signal gain, and therefore implicitly also by the frequency.

At this point the actual values of V_K and V_{GG} can be re-introduced into the formula for V_{dc}, and the procedure repeated; however, if the first guess was close to the final result as is usually the case, only negligible readjustments are found. The design is therefore completed.

CONCLUSIONS

A novel design-oriented analysis method together with design tables and guidelines have been presented, based on a simplified device model. A procedure has been given for the optimum choice of the operating class, and for the determination of bias point, load and drive level. Good agreement has been found with the results of a more elaborate non-linear CAD analysis program and with experimental data.

The computation of the design tables for a selected transistor is quite fast (approx. a minute on a PC) allowing an easy optimization of the power stage.

This work has been carried out within the ESPRIT 6050 - MANPOWER project.

REFERENCES

[1] LIBRA, User's Manual, EEsof Inc., Westlake Village, CA,1992.

[2] Microwave Harmonica, Compact Software Inc., Paterson, NJ, 1992.

[3] Microwave Design System, Hewlett-Packard Co., Palo Alto, CA, 1992.

[4] S.C. Cripps, "A Theory for the Prediction of GaAs FET Load-Pull Power Contours", 1983, IEEE MTT-S Digest, pp. 221-223.

[5] M.G. Adlerstein and M.P. Zaitlin, "Cutoff Operation of Heterojunction Bipolar Transistors", Microwave Journal, n. 9, September 1991, pp. 114-125.

[6] L.J.Kushner, "Output Performance of Idealized Microwave Power Amplifiers",Microwave Journal, n. 10, October 1989, pp. 103-116.

[7] L.J.Kushner, "Estimating Power Amplifiers Large Signal Gain", Microwave Journal, n. 6, June 1990, pp. 87-102.

[8] D.M.Snider, "A Theoretical Analysis and Experimental Confirmation of the Optimally Loaded and Overdriven RF Power Amplifier", IEEE Trans. on ED, Vol. ED-14, Dec. 1967, pp. 851-857.

[9] J.M.Cusack et al., "Automatic load contour mapping for microwave power transistors", IEEE Trans. on MTT, vol.22, no.12, Dec.1974, pp.1146-1152.

[10] F.N. Sechi, "Design Procedure for High-Efficiency Linear Microwave Power Amplifiers", IEEE Trans. on MTT, vol.28, no.11, November 1989, pp.1157-1163.

[11] B.D.Geller, P.E.Goettle, "Quasi-monolithic 4-GHz power amplifiers with 65-percent power-added efficiency", IEEE MTT-S Digest, 1988, New York, pp. 835-838.

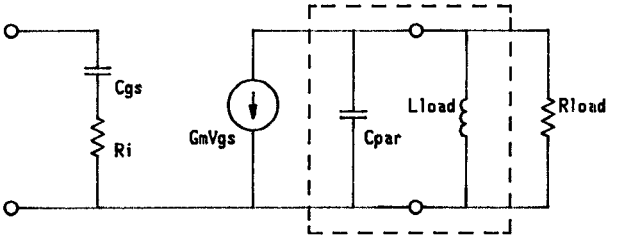


Fig. 1 The output tuned circuit

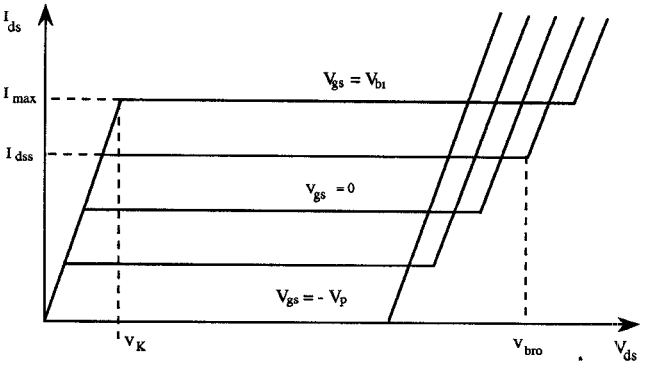


Fig. 2 The output characteristics with the most important design quantities indicated

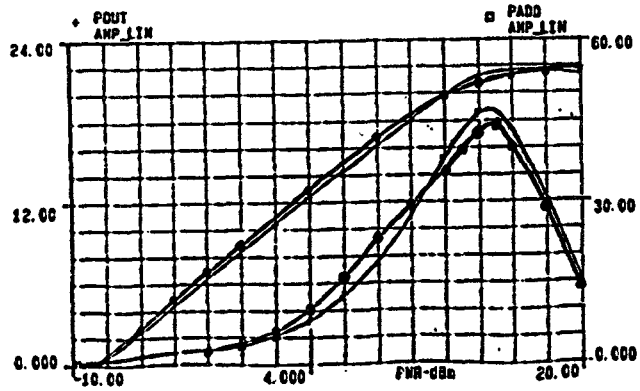


Fig. 3 Comparison between LIBRA (solid line) and our method (dotted): Output Power, PAE

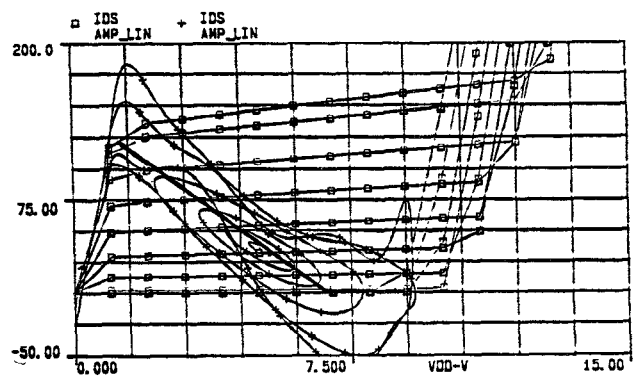


Fig. 4 The load curves for several drive levels (from LIBRA)

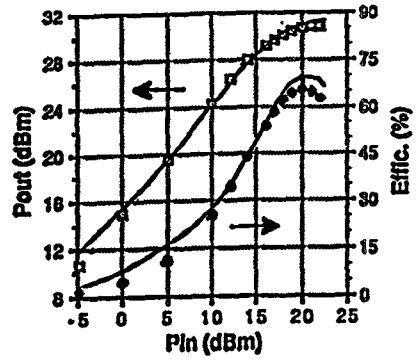
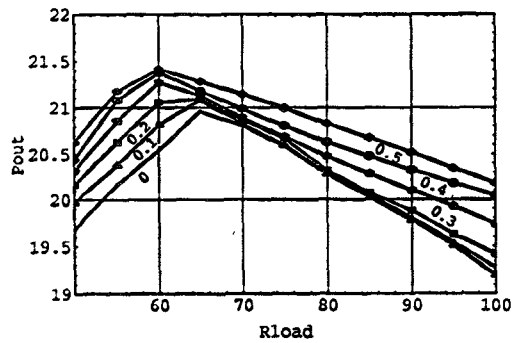
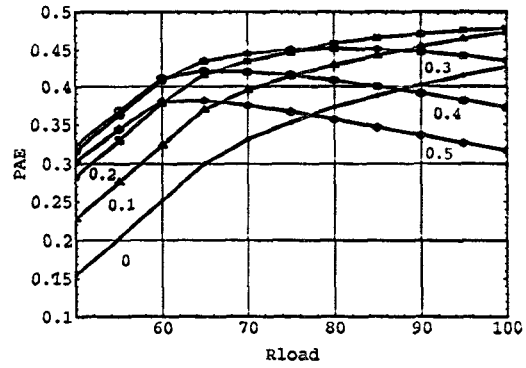
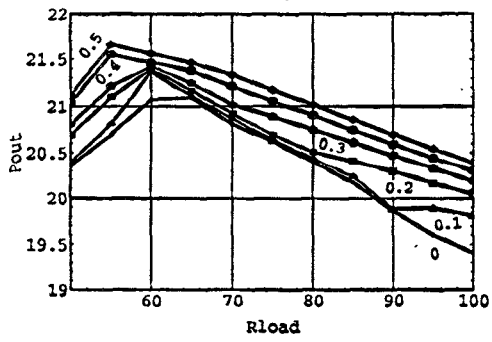


Fig. 5 Comparison between the simplified method (solid line) and experimental results (from [11])



Gain =9 dB





Gain = 15 dB

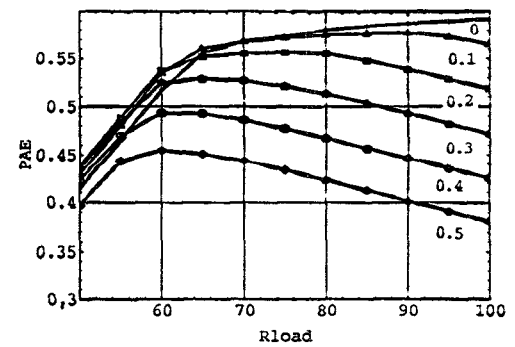


Fig. 6 Output power for a device exhibiting 9 and 15 dB Gain vs. R_L for different bias points (I_{bias}/I_{max})

Fig. 7 Power-added efficiency for a device exhibiting 9 and 15 dB Gain vs. R_L for different bias points (I_{bias}/I_{max})